IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

FLASH-CONTROL LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Civil Action No. 1:19-cv-1107-ADA

JURY TRIAL DEMANDED

PLAINTIFF FLASH-CONTROL LLC'S RESPONSIVE SUMMARY JUDGEMENT AND CLAIM CONSTRUCTION BRIEF

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TABLE OF CONTENTS

I. INTRODUCTION 1

II. SUMMARY OF ARGUMENT 1

III. LEGAL STANDARDS 3

A. Summary Judgement 3

B. Written Description 3

C. Indefiniteness 4

IV. ARGUMENT 5

A. The Specification Satisfies the Written Description Requirement for the Claim Limitation "a second buffer configured to receive information associated with one or more write requests, said write requests being associated with one or more changes to one or more portions of a page in said [non-volatile / NAND flash] memory, said one or more portions being less than the entirety of said page" 5

B. The Specification Provides Written Description Support for the Claim Limitation "locate in said first buffer said one or more portions of said page associated with said one or more write request, and to selectively write said one or more portions to said volatile memory without writing the entirety of said page in said fist buffer to said volatile memory" 8

C. The Specification Provides Written Description Support for the Claim Limitation "to write said one or more changes from said second buffer to said volatile memory, thereby updating said one or more updated portions from said volatile memory to said first buffer, thereby updating said page stored therein to include said one or more changes associated with said one or more write requests" 9

D. Claim 1 of the '880 Patent is Not Indefinite and Should be Given its Plain and Ordinary Meaning 12

V. CONCLUSION 18

TABLE OF AUTHORITIES

Cases

Ariad Pharmaceuticals, Inc. v. Eli Lilly and Co.,
598 F. 3d 1336 (Fed. Cir. 2010) 2, 3

Atmel Corp. v. Info. Storage Devices,
198 F.3d 1374 (Fed. Cir. 1999) 3

Berkheimer v. HP Inc.,
881 F.3d 1360 (Fed. Cir. 2018) 4

Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.,
541 F.3d 1115 (Fed. Cir. 2008) 4

CCS Fitness, Inv. v. Bruswick Corp.,
288 F. 3d 1359 (Fed. Cir. 2002) 3

Celotex Corp. v. Catrett,
477 U.S. 317 (1986) 3

Chi. Bd. Options Exch., Inc. v. Int'l Sec. Exch., LLC,
748 F.3d 1134 (Fed. Cir. 2014) 4

Energizer Holdings v. International Trade Com'n,
435 F.3d 1366 (Fed. Cir. 2006) 16

Hitkansut LLC v. United States,
130 Fed. Cl. 353 (2017) 1

Honeywell Int'l Inv. v. ICM Controls Corp.,
45 F. Supp. 3d 969 (D. Minn. 2014) 17

H-W Tech., L.C. v. Overstock.com, Inc.,
758 F.3d 1329 (Fed. Cir. 2014) 17

In re Gardner,
427 F.2d 786 (CCPA 1970) 4, 15

Loom Co. v. Higgins,
105 U.S. 580 (1881) 4

MOBA, BV v. Diamond Automation, Inc.,
325 F. 3d 1306 (Fed. Cir. 2003) 3

Nautilus, Inc. v. Biosig Instruments, Inc.,
572 U.S. 898 (2014) 4

Scott v. Harris,
550 U.S. 372 (2007) 3

Tech Pharm Servs., LLC v. Alixa Rx LLC,
2016 U.S. Dist. LEXIS 149556 (E.D. Tex. Oct. 28, 2016) 4

Traxcell Techs., LLC v. AT&T, Inc.,
2019 U.S. Dist. LEXIS 64003 (E.D. Tex. Apr. 15, 2019) 4

I. INTRODUCTION

Plaintiff Flash-Control, LLC ("Flash-Control") respectfully submits this Responsive Summary Judgment and Claim Construction Brief in opposition to Defendant Intel Corporation's ("Intel") Motion for Summary Judgment and Opening Claim Construction Brief, (D.I. 48). For the reasons discussed below, Intel's motion should be denied.

II. SUMMARY OF ARGUMENT

Intel has not met its burden for summary judgment. Intel ignores evidence demonstrating the validity of the claims of U.S. Patent Nos. 8,531,880 ("'880 patent," Ex. 1[1]) and 8,817,537 ("'537 patent," Ex. 2) (collectively "patents in suit"[2]). Thus, in view of this evidence there is, at a minimum, a genuine dispute of material fact as to the Intel's assertions of invalidity.

First, Intel wrongly alleges that the patents in suit fail to satisfy the written description requirement of 35 U.S.C. § 112, ¶1[3]. Indeed, there is ample evidence for a jury to render a

[1] Citations to Exhibits in this brief refer to the Exhibits attached to the co-filed Declaration of Derek Dahlgren in Support of Plaintiff Flash-Control, LLC's Responsive Summary Judgment and Claim Construction Brief ("Dahlgren Declaration").

[2] The patents in suit both claim priority back to the same US provisional patent application filed on October 24, 2007, US Prov. Serial No. 60/982,175, and the same US non-provisional utility patent application filed on October 22, 2008, U.S. Patent App. Serial No. 12/256,362, ("the '362 App."). For convenience, this brief refers to the original disclosures of the '362 App. as the "shared specification" and refers to same to show the existence of the requisite support in the original written description of the patents in suit.

[3] Section 112 of the patent laws was amended by Subsection 4(c) of the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 296 (2011). Pursuant to subsection 4(e) of the AIA, the "effective date" of the changes to Section 112 apply to any patent application filed on or after September 16, 2012. *Hitkansut LLC v. United States*, 130 Fed. Cl. 353, 367 n.11 (2017). The continuation patent application for the '880 patent was filed on April 27, 2012, thus the application for the '880 patent and those from which it claims priority were filed before the effective date. The application for the '537 patent, which is a continuation of the application for the '880 patent, was filed on August 15, 2013, after the effective date, but all applications from which it claims priority were filed before the AIA effective date. In any event, the only changes relevant here are the renumbering of paragraphs one through six of Section 112 to subsections (a) through (f), respectively. For simplicity, this brief refers to the relevant paragraphs as originally numbered before enactment of the AIA, i.e., "¶1" (written description) and "¶2" (indefiniteness).

verdict in Flash-Control's favor. Moreover, the issuance of a patent also creates a presumption that the written description requirement is satisfied *Ariad Pharmaceuticals, Inc. v. Eli Lilly and Co*., 598 F. 3d 1336, 1354 (Fed. Cir. 2010) ("A patent is presumed to be valid, and this presumption only can be overcome by clear and convincing evidence to the contrary."). Intel cannot overcome that presumption nor the weight of evidence in Flash-Control's favor.

Intel's litigation-based challenge boils down to the assertion that there is not any disclosure for "moving and modifying a portion of a page in memory." (D.I. 48 at 2.) That is wrong; there is ample support. For example, the specification discloses address decoding, which allows one to locate and modify portions of a page. (Ex. 1 at 2:1-3 ("address decoding circuitry for independent accessible access (read, write etc) at a fine grain level of a bit, or byte.").) Pages in memory are composed of bits and bytes, thus this exemplary disclosure shows that Intel's assertion is wrong. As explained in more detail below, this and other disclosures provide more than ample evidence of adequate written description support in the patents in suit.

Second, Intel alleges that claim 1 of the '880 patent is indefinite because it encompasses three ways of updating the page data stored in the first buffer. Again, not so. The language of the claim is clear on its face and in view of the intrinsic record. The claim refers to "updating said one or more updated portions from said volatile memory . . . ." A person of skill in the art would have understood that this refers to the said one or more portions of the page associated with the write request changes that were previously written to the volatile memory in the preceding limitation. The claim is clear that the changes being written to the one or more portions of the page are what cause the updating—a person of skill in the art would have readily understood that. Intel's litigation-based argument to the contrary is wrong and fails to meet the burden of clear and convincing evidence required to invalidate under Section 112, ¶2.

III. LEGAL STANDARDS

A. Summary Judgement

Summary Judgment may only be granted when there is no genuine dispute of material fact. *Celotex Corp. v. Catrett,* 477 U.S. 317, 323 (1986) ("The Federal Rules of Civil Procedure have for almost 50 years authorized motions for summary judgment upon proper showing of lack of a genuine, triable issues of material fact."). The burden to show there is no genuine dispute as to any material fact lies with the moving party. *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986). In deciding a motion for summary judgment all facts must be viewed in the light most favorable to the nonmoving party. *Scott v. Harris*, 550 U.S. 372, 1775 (2007). Indeed, summary judgment is meant to eliminate unsupported claims or defenses, not preemptively eliminate issues that are properly decided by a jury. *Celotex Corp. v. Catrett,* 477 U.S. 317, 324 (1986).

B. Written Description

Whether the written description requirement is satisfied is a question of fact and the party challenging the claims must prove its case by clear and convincing evidence. *Ariad Pharms., Inc. v. Eli Lilly and Co*., 598 F.3d 1336, 1355 (Fed. Cir. 2010). Section 112, ¶1 requires that the patentee provides adequate support for the claims—nothing more. *MOBA, BV v. Diamond Automation, Inc.,* 325 F. 3d 1306,1319 (Fed. Cir. 2003) ("The question raised by these situations is most often phrased as whether the application provides adequate support for the claims (s) at issue.") (internal quotations omitted). Exhaustive disclosures are not required. *Ariad*, 598 at 1352 ("the written description requirement does not demand either examples or an actual reduction to practice"); *CCS Fitness, Inv. v. Bruswick Corp*., 288 F. 3d 1359, 1366 (Fed. Cir. 2002) ("our case law makes clear that a patentee need not describe in the specification every conceivable and possible future embodiment of his invention.") (internal quotations omitted); *Atmel Corp. v. Info. Storage Devices*, 198 F.3d 1374, 1385 (Fed. Cir. 1999) (specification does

not need to include material known to a person of skill in the art because "'that which is common and well known is as if it were written out in the patent and delineated in the drawings.'") (quoting *Loom Co. v. Higgins*, 105 U.S. 580, 586 (1881)). The specification need only allow a person of ordinary skill in the art to recognize that the patentee invented what is claimed. *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008).

C. Indefiniteness

As mandated by 35 U.S.C. § 112, ¶2 "patent claims, viewed in light of the specification and prosecution history, [are required to] inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). This standard requires clarity. *Id.* at 910. The law recognizes that "absolute precision is unattainable." *Id.* at 910. Additionally, a claim is not indefinite simply because it is broad in scope. *In re Gardner*, 427 F.2d 786, 788 (CCPA 1970) ("Breadth is not indefiniteness."). Nor does all language in a claim qualify as an actual limitation. *Tech Pharm Servs., LLC v. Alixa Rx LLC*, 2016 U.S. Dist. LEXIS 149556, at *54-55 (E.D. Tex. Oct. 28, 2016). In such cases, courts will reject an indefiniteness argument based on the nonlimiting phrase. *See id*. at *55.

The party challenging validity based on indefiniteness carries the burden of proof. *Chi. Bd. Options Exch., Inc. v. Int'l Sec. Exch.*, LLC, 748 F.3d 1134, 1141 (Fed. Cir. 2014). This requires the challenger to establish any fact that is critical to a holding of indefiniteness by clear and convincing evidence. *One-E-Way, Inc.*, 859 F.3d at 1062; *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1368 (Fed. Cir. 2018). As a result, courts should be wary of conclusory expert testimony proffered in support of indefiniteness arguments. *Traxcell Techs., LLC v. AT&T, Inc.*, 2019 U.S. Dist. LEXIS 64003, at *75 (E.D. Tex. Apr. 15, 2019) (rejecting conclusory expert testimony that was contradicted by the intrinsic record); *Phillips*, 415 F.3d at 1318 ("extrinsic evidence

consisting of expert reports and testimony is generated at the time of and for the purpose of litigation and thus can suffer from bias.").

IV. ARGUMENT

A. The Specification Satisfies the Written Description Requirement for the Claim Limitation "a second buffer configured to receive information associated with one or more write requests, said write requests being associated with one or more changes to one or more portions of a page in said [non-volatile / NAND flash] memory, said one or more portions being less than the entirety of said page"

The shared specification provides support for this claim limitation, (Ex. 1 at 5:1-6). First, contrary to Intel's suggestion (D.I. 48 at 14), the specification provides support for the claimed second buffer in multiple places. For example, the page buffer (shown in green) in Figure 9 may act as the first buffer and the read/write buffer (shown in yellow) may act as the second buffer.

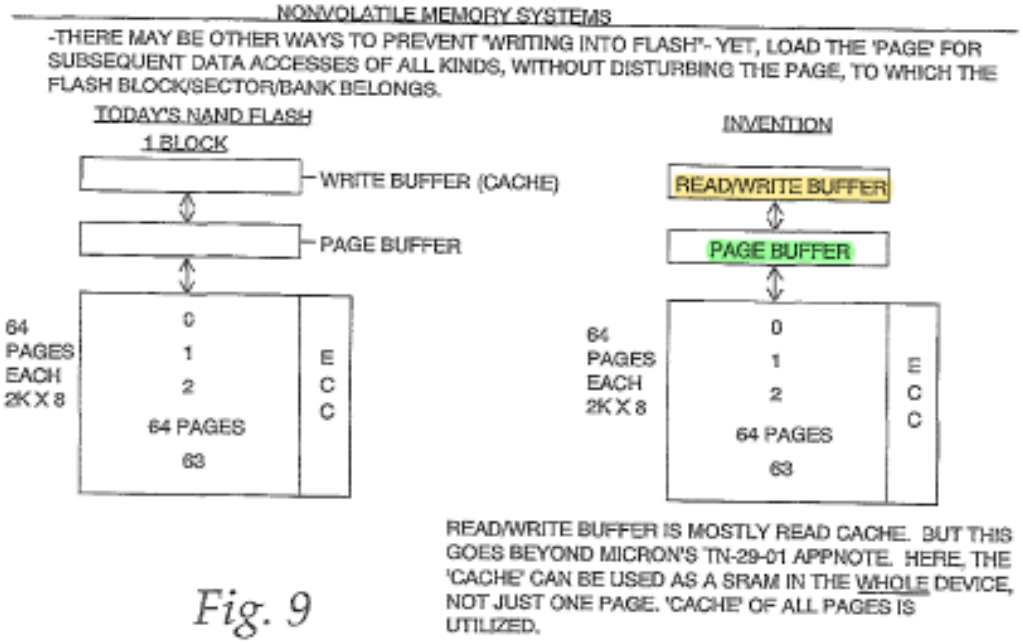

Fig. 9

(Ex. 3 at ¶35[4]; Ex. 4 at 197:3-9.[5])

As shown above, Intel's argument that "there is no figure or description that shows a ***second*** buffer, let alone a second buffer that can store a write request" is wrong on multiple levels.

[4] Exhibit 3 is the Declaration of Dr. Nader Bagherzadeh.
[5] Exhibit 4 is excerpts of testimony from the deposition of Dr. Carl Sechen, dated April 10, 2020.

(D.I. 48 at 14 (emphasis in original); Ex. 3 at ¶35.) As illustrated in Figure 9, there is clearly a disclosure of two buffers, *i.e.*, a first and second buffer. Moreover, Intel confuses the claim by suggesting the second buffer must store the write request. (D.I. 48 at 14.) Not so. The claim refers to the second buffer receiving information ***associated*** with one or more write requests. The actual write request could be stored elsewhere. (Ex. 3 at ¶35.)

The shared specification contains additional support for the claimed second buffer. For example, a second buffer is present in Figure 6. (Ex. 3 at ¶37.) Figure 6 shows a data register and a cache register. (Ex. 1 at Fig. 6.) Registers can be synonymous with buffers. (Ex. 3 at ¶37; Ex. 4 at 161:1-4.) Therefore, those two registers provide support for two buffers and the patents expressly state that the invention involves, in part, "modify[ing] the already existing 'buffers,'" (Ex. 1 at 1:63-64.). A person of skill in the art would have understood this. (Ex. 3 at ¶37.)

Next, Intel challenges the shared specification's support for the remainder of this claim limitation, *i.e.*, the 'configuration' features of the "second buffer". As a threshold matter, contrary to Intel's assertion, the claim does not call for "writing a partial page to non-volatile memory," (D.I. 48 at 15 (citing Sechen Declaration, D.I. 48-10 at ¶¶55-57)), but rather "to receive information associated with one or more write requests . . . associated with one or more changes to one or more portions of a page in . . . [non-volatile / NAND flash] memory." (Ex. 1 at 5:1-6; Ex. 2 at 5:4-9.) The configuration features of this claim limitation are well supported.

First, the patents in suit also disclose that:

> [t]he invention described in this utility patent application focuses on ways to modify the already existing "buffers" in an optimal manner to enhance the random access performance of nonvolatile IC, subsystem and system. The volatile random access memory (RAM) in a preferred embodiment is a 6-transistor SRAM memory cell at the core, ***and complete peripheral address decoding circuitry for independent accessible access (read, write etc) at a fine grain level of a bit, or byte***.

(Ex. 1 at 1:63-2:3.[6]) Address decoding is used by computer systems to decode the addresses on the address bus to the select memory locations in one or more memory or peripheral devices. (Ex. 3 at ¶39.) It generally involves the use of decoders and address registers, the latter which typically store addresses of memory locations. (Ex. 3 at ¶39.) A person of skill in the art would have understood that address decoding, and the address decoding circuitry, allows for the reading and writing of data that is stored in memory, including the reading and writing of data that makes up less than an entire page, *i.e.*, at the more granular level of a bit or byte. (Ex. 1. at 2:1-3; Ex. 3 at ¶39.) Address decoding also would have been understood to be involved in the storage of information associated with write requests, particularly as write request commands generally include information concerning the identity/location of the data that is subject to the write request command. (Ex. 3 at ¶39; *see also* Ex. 4 at 220:7-22113.)

Another example, discussed above, is Figure 9's disclosures of the "read/write" buffer. (Ex. 3 at ¶35 ("The read/write buffer, which acts as the second buffer, provides a mechanism to temporarily store the information associated with write requests, hiding the latency between the processor and providing a more granular capability (finer increments of data) to perform read/write requests.")))

The patents in suit also disclose a buffer with the ability "to receive information associated with one or more write requests" in connection with the disclosure of the data register. (Ex. 3 at ¶38.) For example, as disclosed in connection with Figure 3, a data register (shown as DATA REG) is used as a component "of a controller for the nonvolatile memory system (NVMS) of this invention." (Ex. 1 at 2: 52-53; Ex. 2 at 2:55-56.) One of skill in the art would have understood that a data register is capable of controlling the read/write combinations, allowing it to receive and store the write requests. (Ex. 3 at ¶38.)

[6] Unless indicated otherwise, all emphases in this Brief are added.

B. The Specification Provides Written Description Support for the Claim Limitation "locate in said first buffer said one or more portions of said page associated with said one or more write request, and to selectively write said one or more portions to said volatile memory without writing the entirety of said page in said fist buffer to said volatile memory"

Here, again, there is no genuine dispute that the shared specification provides adequate disclosure. Contrary to Intel's assertions, this limitation has ample written description support. For example, address decoding circuitry as described in the specification allows for "***locat[ing] in [a] first buffer . . . one or more portion of [a] page***". (Ex. 1 at 2:1-3 ("address decoding circuitry for independent accessible access (read, write etc) at a fine grain level of a bit, or byte.").) This allows reading or writing by a bit or a byte, both of which, as Intel's expert acknowledges, are smaller—*i.e.*, portions of—a page. (Ex. 4 at 221:5-13.) Additionally, "since each block (sector) is addressable, one can have a 'Tag address bit' – if enabled it can activate page addressing." (Ex. 1 at 3:29-30.) A tag address bit allows the locating of a bit, *i.e.*, a portion of a page. (Ex. 3 at ¶42.)

As another example, the "switch" disclosed in the shared specification allows for writing to volatile memory. (Ex. 1 at 3:31-34 ("Control page – Nonvolatile array communication with a 'Switch' where volatile and nonvolatile memory can be accessed (unlike current art) – then page 2 Kbytes can be used as independent RAM for other useful purposes."); Ex. 3 at ¶43.) Additional support for writing a portion of a page includes the disclosure that a page "can be read and written (random page access, random access within a page, serial access from a page etc.)." (Ex. 1 at 3:43-48.) The random access ***within a page*** and ***serial access from a page*** are examples of a portion of a page that can be written.

A portion of a page may also be moved by coupling buffers with each block of memory. (Ex. 3 at ¶45.) Intel agrees that coupling allows an entire page to be moved. (D.I. 48 at 15.) But as Intel fails to mention, it also allows a portion or portions of a page to be moved. (Ex. 3 at

¶45.) Intel argues that this coupling does not relate to the claims. (D.I. 48 at 15 citing Sechen Declaration, D.I. 48-10 at ¶¶55-63.) Not so. Coupling a buffer to each block of memory and enabling entire pages to be moved does not prevent or limit portions of a page from being moved as recited in this limitation—both are included within the understanding of coupling for a person of ordinary skill. (Ex. 3 at ¶45.)

Additionally, the commands Intel points to, "read byte out of page" and "write byte out of page," provide further support. A person of ordinary skill in the art would have recognized this. As Dr. Bagherzadeh points out, a person of ordinary skill in the art would have understood that the use of these commands is for reading and writing byte(s) (*i.e.* portions) out of a page. (Ex. 3 at ¶46; *see also* D.I. 48-10 at 6-7 (acknowledging bytes are portions of a page).) Intel's attempt to argue that these commands nonetheless fall short of meeting the written description requirement is entirely without merit.

C. The Specification Provides Written Description Support for the Claim Limitation "to write said one or more changes from said second buffer to said volatile memory, thereby updating said one or more updated portions from said volatile memory to said first buffer, thereby updating said page stored therein to include said one or more changes associated with said one or more write requests"

The shared specification provides adequate support for this claim limitation. Here, the patents in suit show possession of the concept of using the second buffer and modifying a portion of a page. (Ex. 3 at ¶¶47-51.) For example, as evidenced in the reproduction above, Figure 9 shows a page buffer (with green highlighting added), which may act as the first buffer, and the read/write buffer (with yellow highlighting added), which may act as the second buffer. (Ex. 3 at ¶¶35, 48.)

The shared specification further discloses, in certain embodiments, a page buffer and write cache buffer, which may act as the first and second buffers, respectively: "The 'page' architecture in NAND indeed has 'static latches' that can temporarily store data as a buffer (one

page per block), and sometimes have an additional 'write cache buffer for the whole IC." (Ex. 1 at 1:49-53; Ex. 3 at ¶¶35, 48.) A person of ordinary skill in the art would further have understood that in some instances, the page buffer and write cache buffer may be adapted to serve as first and second buffers. (Ex. 3 at ¶¶36, 48.)

The shared specification provides further support for modifying a portion of a page by disclosing a switch that may access volatile and nonvolatile memory to move a portion of a page. (Ex. 1 at 3:31-34 ("Control page – Nonvolatile array communication with a 'Switch' where volatile and nonvolatile memory can be accessed (unlike current art) then page 2 Kbytes can be used as independent RAM for other useful purposes."); Ex. 3 at ¶¶43, 50.)

The ability to modify a portion of a page is further supported by the ability to read and write random access within a page and serial access for a page. (Ex. 3 at ¶51.) The shared specification discloses that "a page . . . can be read and written (random page access, random access within a page, serial access from a page etc.)." (Ex. 1 at 3:43-48.) A person of skill in the art would have understood that "access within a page" includes reading and writing a portion of a page because something within a page is smaller—*i.e.*, a portion of—a page. (Ex. 3 at ¶¶38, 52.) In fact, as noted throughout this brief, the specification particularly points out the bit by bit or byte by byte ability to read and write within a page. (Ex. 1 at 2:2-3 ("independent accessible access (read, write etc) at a fine grain level or a bit, or byte.").)

In addition, as noted above, Figure 3 describes a controller with a data register ("Data Reg"), providing further § 112 support. (Ex. 3 at ¶¶38, 52.) The data register is capable of controlling read/write combinations, thus, allowing movement and/or modification of pages or portions thereof. (Ex. 3 at ¶¶38, 52.) Additionally, the data register may be used as a read buffer and/or a write buffer. (Ex. 3 at ¶¶38,52.) This also allows modifying a portion of a page, and more. (Ex. 3 at ¶¶38,52.)

Intel's assertion that the specification does not provide sufficient support for the claimed "changes," *i.e.*, changes to a portion of a page, is incorrect. The specification provides ample support for changes to a portion of a page. As mentioned above, the specification describes bit by bit or byte by byte reading and writing. (Ex. 1 at 2:2-3 ("independent accessible access (read, write etc) at a fine grain level or a bit, or a byte.").) Writing at a "fine grain level" provides support for changes to a portion of a page. (Ex. 3 at ¶¶39, 44.) Writing creates a change in the data, and the fine grain level or bit or byte is a portion of a page. (Ex. 3 at ¶¶39, 44.) Thus, this indisputably refers to ***making a change to a portion of a page***. (Ex. 3 at ¶¶39, 44.) Intel's expert, Dr. Sechen, when questioned about this disclosure stated that it was not referring to any invention disclosed in the patent. (Ex. 4 at 225:7-229:10.) That is wrong. This disclosure expressly states that this is a preferred embodiment. (Ex. 1 at 1:67.)

Furthermore, the shared specification discloses that "a page of the currently unused block's page…can be read and written (random page access, random access within a page, and serial access from a page etc.)." (Ex. 1 at 3:46-48.) Random access within a page and serial access form a page are examples of a portion of a page. (Ex. 3 at ¶¶¶44, 51, 55; Ex. 4 at 216:24-217:13.) The shared specification says that these portions of a page may be read or written, and writing is making a change.

Intel agrees that coupling buffers with each block of memory allows moving an entire page. (D.I. 48 at 15.) It also allows for more than just moving an entire page, which Intel fails to acknowledge. As mentioned above, coupling buffers allows moving portions of a page as well. (Ex. 3 at ¶45.) That is, coupling a buffer to each block of memory and enabling entire pages to be moved does not, as Intel suggests (D.I 48 at 15 citing Sechen Declaration, D.I. 48-10 at ¶¶55-63), prevent or limit ***portions*** of a page from also being moved (Ex. 3 at ¶53).

As discussed above, Intel incorrectly asserts that the commands "read byte out of page" and "write byte out of page" fall short of meeting the written description requirement. A person of ordinary skill in the art would have understood these commands to refer to reading and writing portions of a page. (Ex. 3 at ¶¶46, 54.) As such these commands demonstrate that a person of ordinary skill in the art would have understood the patentee was in possession of this claim limitation.

Intel's arguments that there is no supporting disclosure is based on a fundamental misunderstanding of the patents in suit. Dr. Sechen repeatedly stated that various embodiments of the invention were supposedly not related to this claim limitation. (Ex. 4 at 226:19-228:25 (stating in part "Well, there is no invention in the column 1 to column 2 thing we're talking about. This is discussing conventional prior art RAM, SRAM architecture right? That's not a – that's not an invention. And - - ***and so that is not related to claim 1***, limitation 4 . . . No, ***this embodiment*** is from the '916 and '452 patents. ***It's got nothing to do with claim 1*** here.").) But the disclosure he was discussing indisputably refers to embodiments of the invention:

> ***The invention described in this utility patent application*** focuses on ways to modify the already existing "buffers" in an optimal manner to enhance the random access performance of nonvolatile IC, subsystem and system. The volatile random access memory (RAM) ***in a preferred embodiment*** is a 6-transistor SRAM memory cell at the core, and complete peripheral address decoding circuitry for independent accessible access (read, write etc) at a fine grain level of a bit, or byte.

(Ex. 1 at 1:63-2:3.) Dr. Sechen's opinions are further flawed because he based them on his belief that the ***"volatile memory"*** referred to in the above section of the specification is different than the ***"volatile memory"*** recited in claim 1 of the '880 patent—even though the terms are identical. (Ex. 4 at 238:16-21.) His blinkered and flawed opinions cannot rise to the level of clear and convincing evidence to support invalidating the patents in suit.

D. Claim 1 of the '880 Patent is Not Indefinite and Should be Given its Plain and Ordinary Meaning

Disputed Claim Term or Phrase	Plaintiff Flash-Control's Proposed Construction	Defendant Intel's Proposed Construction
"thereby updating said one or more updated portions from said volatile memory to said first buffer" (claim 1 of the '880 patent)	Plain and ordinary meaning.	Indefinite

The phrase "thereby updating said one or more portions from said volatile memory to said first buffer" is not indefinite. A person of ordinary skill in the art would have readily understood the scope of this term. The claim recites, in pertinent part:

> A memory system comprising . . .
>
> a second buffer configured to receive ***information associated with one or more write requests***, said ***write requests being associated with one or more changes to one or more portions of a page*** in said non-volatile memory, said one or more portions being less than the entirety of said page;
>
> . . .
>
> said system further adapted to locate in said first buffer ***said one or more portions of said page associated with said one or more write requests***, and to ***selectively write said one or more portions to said volatile memory*** without writing the entirety of said page in said first buffer to said volatile memory;
>
> said system further adapted to ***write said one or more changes from said second buffer*** to said volatile memory, ***thereby updating said one or more updated portions from said volatile memory to said first buffer***, thereby updating said page stored therein to include said one or more changes associated with said one or more write request; and
>
> said system further adapted to write said updated page from said first buffer to an erased page in said non-volatile memory.

(Ex. 1 at 4:62-5:27). Intel argues this limitation is indefinite because it encompasses three different ways for updating the page in the first buffer. Only one is correct. And Intel identifies the proper scope in the first of its alternatives: "the changes that were written to the volatile memory in the prior step be written to the first buffer."

Here, a person of skill in the art would have understood that "said one or more updated portions" refers to the said one or more portions of the page associated with the write request(s) that were previously written to the volatile memory in the preceding limitation. (Ex. 3 at ¶¶57-59.) A person of skill in the art would also have understood in the claim that writing a change to one or more portions of the page is what results in the updating. (Ex. 3 at ¶¶57-59.) Thus, the claim would have indicated to one of skill in the art that by writing changes from the second buffer to the volatile memory, it results in the first buffer being updated with those changes (*i.e.* updates). (Ex. 3 at ¶¶57-59.)

A person of ordinary skill in the art would ***not*** have understood that the claim covers updating a portion of the page, the entirety of the page, or the page plus more data. (Ex. 3 at ¶58.) Claim 1 of the '880 patent recites "thereby updating said one or more updated portions from said volatile memory to said first buffer." (Ex. 1 at 5:11-27.) The claim refers to "changes to one or more portions of a page," which are associated with "write requests." (Ex. 1 at 5:2-4.) The "updates" are associated with these "changes." (Ex. 1 at 5:18-20.) Because of the clear the relationship between "write requests," "changes," and "updates," a person of skill in the art would have readily understood "updating said one or more updated portions" refers to the "one or more changes to one or more portions of a page in said non-volatile memory" that are "associated with" the "write requests" that are "associated with" the "one or more changes" that are "receive[d]" by the "second buffer," and written to the volatile memory, as recited in the fourth clause of claim 1. (Ex. 3 at ¶¶57-59.) A person of skill in the art would have understood this with reasonable certainty.

Intel's contrary arguments are simply wrong. A person of skill in the art would ***not*** have understood that the "updating" at issue refers to those changes recited in the claim as well as additional information stored in the volatile memory or only a subsection of the changes. (Ex. 3

at ⁋59.) Neither of these alternatives is plausible. (Ex. 3 at ⁋⁋57-59.) A person of skill in the art would have readily ascertained that "said one or more updated portions" refers to the said one or more portions of the page associated with the write request(s) that were previously written to the volatile memory in the preceding limitation. Additionally, the claim language indicates that writing a change to the page is what results in the updating. Thus, the claim clearly indicates—and would have informed a person of skill in the art—that the change results in the first buffer being updated with the changes associated with the write requests. (Ex. 1 at 5:11-27.)

Nor would the claim even be indefinite under Intel's construction that there are supposedly three different ways or updating. A claim encompassing three (or even more) ways of updating a page is not indefinite, ambiguous, or in any way not understandable. "Breadth is not indefiniteness." *In re Gardner*, 427 F.2d 786, 788 (CCPA 1970). While Intel and its expert are mistaken about their construction, Intel's expert, Dr. Sechen, nonetheless agreed that one of skill in the art would have understood the claim to include these three options. (Ex. 4 at 15:4-10)

Intel also incorrectly argues, without legal basis, that claim 1 of the '880 patent is indefinite due to an alleged failure to use functional language. Intel asserts that "[t]he claim, as published, is indefinite because it fails to functionally describe how the first buffer is updated." (D.I. 48 at 18.) Intel's brief proceeds to morph this 'functional deficiency' argument over how 'updating' functionally occurs, to an assertion that claim 1 of the '880 patent is fatally defective for not clearly specifying ***what*** is updated. This contorted position by Intel was not clear at the time of Plaintiff simultaneously filed Opening Claim Construction Brief.[7] Therefore, Plaintiff's Opening Brief focused on a patentee's right to broadly claim a function such a 'updating'

[7] Plaintiff's original Opening Claim Construction Brief (D.I. 49) was filed simultaneously with Intel's combined claim construction brief and motion for summary judgment (D.I. 48). Plaintiff's original brief has since been mooted. In a docket text ORDER issued March 15, 2020, the Court adopted a revised briefing scheduling setting April 20, 2020 as Plaintiff's new deadline to submit a "Combined responsive CC and MSJ Brief."

broadly. (D.I. 49 at 9-10) Notably, Intel's brief acknowledges that "updating" essentially refers to 'writing,' in functional terms. (D.I. 48 at 18 ("Without instructions on how the first buffer is updated, . . . there are multiple possible ways this step could be carried out. In one potential interpretation . . . changes . . .***written*** to the first buffer. In another interpretation, . . . changes . . . ***written*** to the first buffer. And in yet a third interpretation, . . . changes might be moved . . . a selective ***write operation***.") (emphasis added).)

Intel alleges that a person of ordinary skill in the art would have been left in the dark about the scope of the claim because there are multiple alternative ways in which changes could be updated from the volatile memory to the first buffer. But Intel is again mistaken. Intel's confusion appears to stem from its refusal to recognize the antecedent basis of the word "***said***" appearing in the phrase "thereby updating ***said*** one or more updated portions." (Ex. 1 at 5:20-21; D.I. 48 at 20 ("The uncertainty as to the scope of the claim is exacerbated by the fact that the limitation "said one or more updated portions" is missing an antecedent basis").) But "antecedent basis can be present by implication." *Energizer Holdings v. International Trade Com'n,* 435 F.3d 1366, 1371 (Fed. Cir. 2006).

Here, a person of skill in the art would have readily understood the implicit antecedent for "***said one or more updated portions***". A person of skill in the art would have understood this to refer to the said one or more portions of the page associated with the write request(s) that were previously written to the volatile memory and then changed with data from the second buffer in the preceding limitation. (Ex. 3 at ¶57.) The claim clearly indicates that writing a change to one or more portions of the page is what results in the updating. Thus, the claim clearly indicates that the change results in the first buffer being updated with the changes associated with the write requests. (Ex. 3 at ¶¶57-59.)

Intel's 'multiple alternatives' view is wrong on many levels. First, Intel is wrong to refer, in its first alternative, to a "prior step", because claim 1 is not a method claim. If nothing else, this reveals that Intel is misconstruing this claim. Second, the fact that Intel focuses on "***changes***" within each of its three alternatives reveals that Intel, by *implication*, recognizes that "***updates***" are a corollary to "***changes***" and the claim itself literally "associate[s]" these "***changes***" with "***write requests***". Thus, "***updates***" are to be associated with "***write requests***" to make one or more "***changes to one or more portions of a page***". (Ex. 1 at 5:1-5.) Third, in view of the corollary between "***write requests,***" "***changes***," and "***updates***" there is an implicit antecedent for the "***said one or more updated portions***" phrase at issue, specifically the "one or more ***changes*** to ***one or more portions*** of a page in said non-volatile memory" that are "associated with" the "write requests" that are "associated with" the "information" that is "receive[d]" by the "second buffer" as recited in claim 1. In sum, it is simply wrong for Intel to suggest that the "updating" at issues refers to "those changes [recited in the claim] as well as additional information stored in the volatile memory" or "only a subsection of the changes." Neither of these alternatives is plausible.

Intel is also misguided in its reliance on *Honeywell Int'l Inv. v. ICM Controls Corp*., 45 F. Supp. 3d 969, 982-84 (D. Minn. 2014). That case involved the Court determining whether the scope of the claim would differ depending on which language was read into the preamble of the claim. *Id.* at 983-34. Here, Intel does not contest that the claim language is broad enough to encompass the three options. It instead seeks to argues that the claim irreconcilably requires finding multiple alternative options for "thereby updating," which must render the claim fatally indefinite. Intel is wrong.

Intel's reliance on *H-W Tech., L.C. v. Overstock.com, Inc.,* 758 F.3d 1329 (Fed. Cir. 2014) is also misplaced. That case involved an inadvertently omitted limitation and whether it

should be read into the claim, and whether the patentee could assert a corrected version of the claim. *Id.* at 1332-34. The Federal Circuit held that the patentee could not assert the original claim and that the District Court could not cure the omission by reading the missing limitation into the claim. *Id.* at 1332-34. Here, even if Intel's implausible theory were adopted, the mere notion that "thereby updating" could have broad scope cannot server to render the claim indefinite. The case is thus inapposite.

V. CONCLUSION

For all the foregoing reasons, Flash-Control respectfully requests that the Court deny Intel's motion for summary judgement because the claimed limitations have adequate support in the shared specification of the patents in suit. Flash-Control additionally requests that the Court find that Intel has not demonstrated that claim 1 of the '880 patent is indefinite and give the disputed term its plain and ordinary meaning.

Dated: April 23, 2020

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CERTIFICATE OF SERVICE

I hereby certify that on April 24, 2020, I caused a copy of this document to be served by transmitting it via e-mail or electronic transmission to counsel of record for Defendant.

/s/ Timothy Devlin
Timothy Devlin